LEADING AT THE EDGE
TECHNOLOGY AND MANUFACTURING DAY
MOORE’S LAW LEADERSHIP

MARK BOHR

Intel Senior Fellow, Technology and Manufacturing Group Director, Process Architecture and Integration
Intel Technology and Manufacturing Day 2017 occurs during Intel's “Quiet Period,” before Intel announces its 2017 first quarter financial and operating results. Therefore, presenters will not be addressing first quarter information during this year's program.

Statements in this presentation that refer to forecasts, future plans and expectations are forward-looking statements that involve a number of risks and uncertainties. Words such as "anticipates," "expects," "intends," "goals," "plans," "believes," "seeks," "estimates," "continues," "may," "will," "would," "should," "could," and variations of such words and similar expressions are intended to identify such forward-looking statements. Statements that refer to or are based on projections, uncertain events or assumptions also identify forward-looking statements. Such statements are based on management's expectations as of March 28, 2017, and involve many risks and uncertainties that could cause actual results to differ materially from those expressed or implied in these forward-looking statements. Important factors that could cause actual results to differ materially from the company's expectations are set forth in Intel's earnings release dated January 26, 2017, which is included as an exhibit to Intel’s Form 8-K furnished to the SEC on such date. Additional information regarding these and other factors that could affect Intel's results is included in Intel's SEC filings, including the company's most recent reports on Forms 10-K, 10-Q and 8-K reports may be obtained by visiting our Investor Relations website at www.intc.com or the SEC's website at www.sec.gov.
KEY MESSAGES

- Intel leads the industry in introducing innovations that enable scaling

- Hyper scaling on Intel 14 nm and 10 nm provides better-than-normal scaling while continuing to reduce cost per transistor

- Intel's 14 nm technology has ~3 year lead over other “10 nm” technologies with similar logic transistor density

- Intel's 10 nm technology provides industry-leading logic transistor density using a quantitative density metric

- Enhanced versions of 14 nm and 10 nm provide improved performance and extend the life of these technologies

Moore’s Law is alive and well at Intel

Source: Amalgamation of analyst data and Intel analysis, based upon current expectations and available information.
Intel leads the industry by at least 3 years in introducing major process innovations.
Intel innovation leadership

Intel leads the industry by at least 3 years in introducing major process innovations

Intel:
- 90nm in 2003
- 65nm in 2004
- 45nm in 2005
- 32nm in 2006
- 22nm in 2007
- 14nm in 2008
- 10nm in 2009

Others:
- 90nm in 2003
- 65nm in 2004
- 40nm in 2005
- 28nm in 2006
- 20nm in 2007
- 16nm in 2008
- 10nm in 2009

Strained Silicon:
- 90nm in 2003
- 65nm in 2004

Source: Intel
Intel leads the industry by at least 3 years in introducing major process innovations.
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Intel leads the industry by at least 3 years in introducing major process innovations.
Intel leads the industry by at least 3 years in introducing major process innovations.
Intel developed all the major logic process innovations used by our industry over the past 15 years.

Source: Intel. 10 nm is based upon current expectations and available information.
## Industry Recognitions

<table>
<thead>
<tr>
<th>Year</th>
<th>Award Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2008</td>
<td>SEMI Award for North America</td>
<td>“For integration of strain-enhanced mobility techniques for CMOS transistors”</td>
</tr>
<tr>
<td>2012</td>
<td>SEMI Award for North America</td>
<td>“For the first development, integration and introduction of a successful high-k dielectric and metal electrode gate stack for CMOS IC production”</td>
</tr>
<tr>
<td>2015</td>
<td>SEMI Award for North America</td>
<td>“For implementation of bulk CMOS FinFET production”</td>
</tr>
<tr>
<td>2016</td>
<td>IEEE Corporate Innovation Award</td>
<td>“For pioneering the use of high-k metal gate and tri-gate transistor technologies in high-volume manufacturing”</td>
</tr>
</tbody>
</table>
Traditional logic area scaling was ~0.49x per generation using a “gate pitch x cell height” metric.
... but “gate pitch x cell height” is not a comprehensive transistor density metric
Standard NAND+SFF metric is a more accurate estimate of logic transistor density

\[
0.6 \times \frac{\text{NAND2 Tr Count}}{\text{NAND2 Cell Area}} + 0.4 \times \frac{\text{Scan Flip Flop Tr Count}}{\text{Scan Flip Flop Cell Area}} = \text{# Transistors / mm}^2
\]
Logic transistor density improvement was ~2.2x per generation using NAND+SFF metric

Source: Intel
14 nm hyper scaling provided ~2.5x transistor density improvement

Source: Intel
10 nm hyper scaling provides ~2.7x transistor density improvement

Source: Intel. 2017-2020 are estimates based upon current expectations and available information.
Transistor density improvements continue at a rate of ~doubling every 2 years.

Source: Intel. 2017-2020 are estimates based upon current expectations and available information.
Logic node names should be accompanied with logic transistor density.

Source: Intel. 2017-2020 are estimates based upon current expectations and available information.
Other measured transistor densities using same NAND+SFF metric

Source: Amalgamation of analyst data and Intel analysis. 2017-2020 are estimates based upon current expectations and available information.
Rate of density improvement was slow on other 20/16/14 nm technologies

Source: Amalgamation of analyst data and Intel analysis. 2017-2020 are estimates based upon current expectations and available information.
Intel 14 nm has ~1.3x higher transistor density than other 20/16/14 nm

Source: Amalgamation of analyst data and Intel analysis. 2017-2020 are estimates based upon current expectations and available information.
Other "10 nm" technologies will have density similar to Intel 14 nm, but ~3 years later.

Source: Amalgamation of analyst data and Intel analysis. 2017-2020 are estimates based upon current expectations and available information.
Logic node names should be accompanied with logic transistor density

Source: Amalgamation of analyst data and Intel analysis. 2017-2020 are estimates based upon current expectations and available information.
MOORE'S LAW IS A LAW OF ECONOMICS

<table>
<thead>
<tr>
<th>LOWER COST</th>
<th>MORE FUNCTIONALITY (more transistors)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Same circuitry in</td>
<td>Twice the number of transistors in</td>
</tr>
<tr>
<td>half the space</td>
<td>same space</td>
</tr>
<tr>
<td>(Feature Neutral)</td>
<td></td>
</tr>
</tbody>
</table>

**MOORE COST $AVINGS**

**MOORE PERFORMANCE**
**Microprocessor Die Area Scaling**

Normal microprocessor die area scaling has been ~0.62x per generation.

<table>
<thead>
<tr>
<th>Technology (nm)</th>
<th>Area (mm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>45</td>
<td>100</td>
</tr>
<tr>
<td>32</td>
<td>62</td>
</tr>
<tr>
<td>22</td>
<td>38.4</td>
</tr>
<tr>
<td>14</td>
<td>23.8</td>
</tr>
<tr>
<td>10</td>
<td>14.8</td>
</tr>
</tbody>
</table>

Source: Intel.
Hyper scaling delivers 0.46-0.43x die area scaling on 14 nm and 10 nm
Normal scaling would have provided poor CPT improvements
COST PER TRANSISTOR

Normal scaling + 450 mm wafers would have provided better CPT

Source: Intel.
Hyper scaling on Intel 14 nm and 10 nm provides lower CPT
Scaled transistors continue to provide improved performance and lower power.

Source: Intel. 2017-2020 are estimates based upon current expectations and available information.
**Technology Enhancements**

14 nm enhancements improve performance and extend technology life.

Source: Intel. 2017-2020 are estimates based upon current expectations and available information.
10 nm enhancements improve performance and extend technology life.
Multiple derivative options offered for each technology generation
Wide range of 14 nm products in volume production on various derivative technologies
HETEROGENEOUS INTEGRATION OPTIONS

- **Multi-Chip Package**
  - Poor density of die-package connections
  - Poor density of die-die interconnects

- **Interposer**
  - Good density of die-interposer connections
  - Good density of die-die interconnects
  - Higher cost of large interposer + thru-silicon vias

- ** Silicon Interposer**
  - Good density of die-bridge connections
  - Good density of die-die interconnects
  - Low cost of small silicon bridges

**EMIB technology provides high density, high bandwidth die-die interconnects**
EMIB technology provides high density, high bandwidth die-die interconnects.
EMBEDDED MULTI-DIE INTERCONNECT BRIDGE

Silicon Die

55 um pitch bumps

130 um pitch bumps

Silicon Bridge
EMBEDDED MULTI-DIE INTERCONNECT BRIDGE

Silicon Bridge

Silicon Die

55 um pitch bumps

130 um pitch bumps

TECHNOLOGY AND MANUFACTURING DAY
EMIB enables dense and cost effective in-package heterogeneous integration
KEY MESSAGES

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