LEADING AT THE EDGE

TECHNOLOGY AND MANUFACTURING DAY
14 NM TECHNOLOGY LEADERSHIP

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Intel’s 14 nm technology is ~1.3x denser than others’ available “20 nm” and “16/14 nm” technologies.

Intel’s 14 nm technology is expected to be similar density to others’ “10 nm” technology but ~3 years ahead.

Intel’s 14 nm transistors have >20% performance leadership compared to others’ available technology.

At the 14 nm technology node, Intel has developed all of the key enablers to hyper scale features and deliver significant CPT benefits.
KEY MESSAGES

- Intel’s 14 nm technology is ~1.3x denser than others’ available “20 nm” and “16/14 nm” technologies.

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14 nm hyper scaling features

14 nm uses aggressive feature scaling to deliver unprecedented 0.37x logic cell area scaling.

Source: Amalgamation of analyst data and Intel analysis, based upon current expectations and available information.
Hyper scaling of 14 nm features provides better-than-normal 0.37x logic area scaling.

Source: Amalgamation of analyst data and Intel analysis, based upon current expectations and available information.
Using NAND+SFF metric, 14 nm provides better-than-normal logic transistor density improvement.

Source: Amalgamation of analyst data and Intel analysis, based upon current expectations and available information.
Intel's 14 nm technology is ~1.3x denser than others' “14/16/20 nm” technologies.

Source: Amalgamation of analyst data and Intel analysis, based upon current expectations and available information.
## 14nm Technology Features

<table>
<thead>
<tr>
<th>Feature</th>
<th>Intel 14 nm</th>
<th>Other “20 nm”</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate Pitch</td>
<td>70 nm</td>
<td>90 nm (1.3x)</td>
</tr>
<tr>
<td>Logic cell height</td>
<td>399 nm</td>
<td>576 nm (1.4x)</td>
</tr>
<tr>
<td>Fin Pitch</td>
<td>42 nm</td>
<td>Planar</td>
</tr>
<tr>
<td>Min Metal Pitch</td>
<td>52 nm</td>
<td>64 nm</td>
</tr>
<tr>
<td>Transistor density</td>
<td>37.5</td>
<td>28.0</td>
</tr>
<tr>
<td>(MTr/mm²)</td>
<td>(1.34x)</td>
<td>(1x)</td>
</tr>
</tbody>
</table>

Introduced at similar time.

Intel 14 nm is ahead of others’ “20 nm” technology on every density metric.

Source: Amalgamation of analyst data and Intel analysis, based upon current expectations and available information.
### 14nm Technology Features

<table>
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<tr>
<th>Feature</th>
<th>Intel 14 nm</th>
<th>Other “20 nm”</th>
<th>Other “16 nm”</th>
<th>Other “14 nm”</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate Pitch</td>
<td>70 nm</td>
<td>90 nm (1.3x)</td>
<td>90 nm (1.3x)</td>
<td>78 nm (1.1x)</td>
</tr>
<tr>
<td>Logic cell height</td>
<td>399 nm</td>
<td>576 nm (1.4x)</td>
<td>480 nm (1.2x)</td>
<td>576 nm (1.4x)</td>
</tr>
<tr>
<td>Fin Pitch</td>
<td>42 nm</td>
<td>Planar</td>
<td>48 nm (1.1x)</td>
<td>48 nm (1.1x)</td>
</tr>
<tr>
<td>Min Metal Pitch</td>
<td>52 nm</td>
<td>64 nm</td>
<td>64 nm</td>
<td>64 nm</td>
</tr>
<tr>
<td>Transistor density</td>
<td>37.5 (1.34x)</td>
<td>28.0 (1x)</td>
<td>29.0 (1.04x)</td>
<td>30.5 (1.09x)</td>
</tr>
</tbody>
</table>

Others introduced ~1 year later.

Intel 14 nm is ahead of others’ “14/16 nm” technology on every density metric.

Source: Amalgamation of analyst data and Intel analysis, based upon current expectations and available information.
Intel’s 14 nm technology is ~1.3x denser than others’ available “20 nm” and “16/14 nm” technologies.

Intel’s 14 nm technology is expected to be similar density to others’ “10 nm” technology but ~3 years ahead.

Intel’s 14 nm transistors have >20% performance leadership compared to others’ available technology.

At the 14 nm technology node, Intel has developed all of the key enablers to hyper scale features and deliver significant CPT benefits.
Others’ “10 nm” technologies expected to have similar density to Intel 14 nm, but ~3 years later.
KEY MESSAGES

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14+ and 14++ enhancements improve performance without increasing capacitance (active power).

Source: Amalgamation of analyst data and Intel analysis. 2017-2021 are estimates based upon current expectations and available information.
FinFET transistors were first introduced at 22 nm and enhanced at 14 nm. Fin pitch and height are optimized for density and performance.
Intel demonstrated leading 14 nm performance in 2015.

Source: Intel.
Intel's 14+ enhancement enables +12% drive current in 2016.

Source: Intel.
World’s Highest Performance Transistors

Intel’s 14++ enhancement enables +23-24% higher drive current in 2017.
WORLD’S HIGHEST PERFORMANCE TRANSISTORS

Intel’s 14++ performance is >20% better than others’ best “14/16 nm”.

Source: Amalgamation of analyst data and Intel analysis, based upon current expectations and available information.
Transistor performance enhanced on an annual cadence.
Intel's 14 nm technology offers a full suite of capabilities for product design needs.
14nm technology offers full range of interconnects

High Performance Client

High Density SoC

Airgap for performance
Key Messages

- Intel’s 14 nm technology is ~1.3x denser than others’ available “20 nm” and “16/14 nm” technologies.

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Source: Amalgamation of analyst data and Intel analysis, based upon current expectations and available information.
Innovations are the key to scaling. Intel drives the development of key breakthroughs. At 14 nm, we have several generations of learning on traditional enablers.
Self-Aligned Double Pattern interconnects first introduced into logic manufacturing by Intel. Key advantage for density and yield.
Self-Aligned patterning allows Intel to use the full range of interconnect pitches.
Other's patterning choices limit interconnect pitch options.
Self-Aligned Patterning allows Intel to have dense interconnects at lower cost.

Source: Amalgamation of analyst data and Intel analysis, based upon current expectations and available information.
Double Patterning leads to clear benefits in process control.
Self-Aligned Patterning leads to process control.

Self-Aligned Patterning has placement control required for high yield.
SELF-ALIGNED PATTERNING LEADS TO PROCESS CONTROL

Self-Aligned Double Patterning

Litho

Spacer deposition
Thickness control ~1 nm

Etch spacer

Clean and Etch

Pitch Division

Litho-Etch-Litho-Etch

Litho #1

Etch #1

Litho #2
Good placement

Etch #2

Pitch division

Litho-Etch-Litho-Etch can yield same pattern.
Self-Aligned Double Patterning

- Litho
- Spacer deposition
  Thickness control $\sim 1 \text{ nm}$
- Etch spacer
- Clean and Etch
- Pitch Division

Litho-Etch-Litho-Etch

- Litho #1
- Etch #1
- Litho #2
  Good placement
- Etch #2
- Pitch division

Or Litho #2
- Etch #2
- Pitch division

LELE process has yield and performance risk with mis-alignment between patterns.
Self-Aligned Patterning leads to process control

Self-Aligned Double Patterning

Single mask to single mask. Alignment can be tightly controlled.

Litho-Etch-Litho-Etch

Single mask to multiple masks. Difficult to control.
14 nm technology delivers significant die scaling. Hyper scaling delivers <0.50x die area scaling on 14 nm.
14 nm hyper scaling ⇒ ~1.4x more units per $ than traditional scaling

450 mm wafer size conversion ⇒ ~1.4x more units per $ than traditional scaling

14 nm hyper scaling delivers the equivalent economic benefit as a wafer size transition.
SUMMARY

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