CONTINUING MOORE’S LAW

MARK BOHR
INTEL SENIOR FELLOW, TECHNOLOGY AND MANUFACTURING GROUP
DIRECTOR, PROCESS ARCHITECTURE AND INTEGRATION
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China Tech and Manufacturing Day 2017 occurs during Intel’s “Quiet Period,” before Intel announces its 2017 third quarter financial and operating results. Therefore, presenters will not be addressing third quarter information during this year’s program.

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Intel innovation leadership

Intel leads the industry by at least 3 years in introducing major process innovations.
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Intel innovation leadership:
- 90nm
- 65nm
- 45nm
- 32nm
- 22nm
- 14nm
- 10nm

Year:
- '03
- '04
- '05
- '06
- '07
- '08
- '09
- '10
- '11
- '12
- '13
- '14
- '15
- '16
- '17
- '18
- '19
- '20

Others:
- 90nm
- 65nm
- 40nm
- 28nm
- 20nm
- 16nm
- 10nm

Technologies:
- Strained Silicon
- High-k Metal Gate
- Self Align Via
- FinFET Transistor

Intel leads by at least 3 years.
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Intel developed all the major logic process innovations used by our industry over the past 15 years.
Traditional logic area scaling was ~0.49x per generation using a “gate pitch x cell height” metric.
Hyper scaling on 14 nm and 10 nm provides better than normal logic area scaling.
... but “gate pitch x cell height" is not a comprehensive transistor density metric
**Logic Transistor Density Metric**

Standard NAND+SFF metric is a more accurate estimate of logic transistor density.

\[
0.6 \times \frac{\text{NAND2 Tr Count}}{\text{NAND2 Cell Area}} + 0.4 \times \frac{\text{Scan Flip Flop Tr Count}}{\text{Scan Flip Flop Cell Area}} = \# \text{ Transistors / mm}^2
\]
Hyper scaling on 14 nm and 10 nm provides better than normal transistor density.
Transistor density improvements continue at a rate of ~doubling every 2 years.
Transistor density improvements continue at a rate of ~doubling every 2 years.
Normal microprocessor die area scaling has been ~0.62x per generation
Hyper scaling delivers 0.46-0.43x die area scaling on 14 nm and 10 nm
Transistor area is scaling faster than normal
Cost per transistor

45 nm
32 nm
22 nm
14 nm
10 nm
7 nm
$ / mm²
(normalized)

Log Scale

45 nm
32 nm
22 nm
14 nm
10 nm
7 nm
mm² / Transistor
(normalized)

$ / mm²
(normalized)

Wafer cost is increasing
Cost per transistor continues to come down
Scaled transistors continue to provide improved performance per watt.
INNOVATION ENABLED TECHNOLOGY PIPELINE

Wide range of options in research to continue Moore's Law
SUMMARY

• Intel leads the industry in introducing innovations that enable scaling

• Hyper scaling on Intel 14 nm and 10 nm provides better-than-normal scaling while continuing to reduce cost per transistor and improve performance per watt

• Intel’s research and development groups are exploring a wide range of novel technology options to continue scaling for the foreseeable future

Moore’s Law is alive and well at Intel