



## Intel® Many Integrated Core (MIC) Architecture – Performance and Programmability

“Moving a code to MIC might involve sitting down and adding a couple lines of directives that takes a few minutes. Moving a code to a GPU is a project.”<sup>2</sup>

– Dan Stanzione,  
Deputy Director at TACC

“By just utilizing standard programming on both Intel® Xeon® processor and Intel® MIC Architecture-based platforms, the performance met multi-threading scalability expectations and we observed near-theoretical linear performance scaling with the number of threads.”

– Hongsuk Yi, Heterogeneous Computing Team Leader,  
KISTI Supercomputing Center

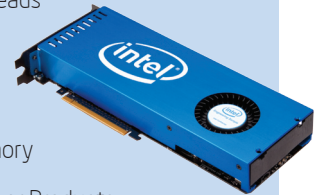
**Delivering breakthrough performance for highly parallel applications and the many benefits of programming to Intel® Architecture with familiar programming models, techniques, and developer tools.**

Relative to the multi-core Intel® Xeon® processors, Intel® MIC Architecture has many more smaller cores, many more hardware threads, and wider vector units. This is ideal for achieving higher aggregate performance for highly parallel applications.

The first Intel® MIC product, codenamed “Knights Corner,” is planned for production on Intel’s 22 nm technology featuring the world’s first 3-D Tri-Gate transistors.<sup>1</sup> Intel is currently shipping software development platforms, codenamed “Knights Ferry,” to selected development partners.

### Knights Ferry Software Development Platform

- Up to 32 cores/128 threads
- 512b SIMD support
- Fully coherent cache
- Up to 2GB GDDR5 memory
- Latest Intel SW Developer Products



### Greater programmer productivity, shorter time to market

As developers embrace high degrees of parallelism (instruction, data, task, vector, thread, cluster, etc.), important and popular programming models for Intel® Architecture processors extend to Intel MIC Architecture without rethinking the entire problem. The same techniques that deliver optimal performance on Intel® processors – scaling applications to cores and threads, blocking data for hierarchical memory and caches, and effective use of SIMD – also apply to maximizing performance on Intel MIC Architecture.

With greater reuse of parallel CPU code, software companies and IT departments benefit from creating and maintaining a single code base binary and not having to re-train developers on proprietary programming models associated with accelerators.

### Get started today!

Optimizing for Multicore with Intel Xeon processors is the best path to make your parallel applications ready for Intel MIC products. Learn more at [intel.com/software/products](http://intel.com/software/products)

<sup>1</sup> [http://newsroom.intel.com/community/intel\\_newsroom/blog/2011/05/04/intel-reinvents-transistors-using-new-3-d-structure](http://newsroom.intel.com/community/intel_newsroom/blog/2011/05/04/intel-reinvents-transistors-using-new-3-d-structure)

<sup>2</sup> [http://www.hpcwire.com/hpcwire/2011-04-21/tacc\\_steps\\_up\\_to\\_the\\_mic.html](http://www.hpcwire.com/hpcwire/2011-04-21/tacc_steps_up_to_the_mic.html)

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