

Intel Announces New Details for Future HPC Products and Extended Industry Collaborations at ISC 2015

ISC2015, Frankfurt, Germany, July 13, 2015 — Intel Corporation today unveiled new details for its future generation high performance computing (HPC) products, including the first public “powered-on” demonstration of the Intel® Omni-Path Architecture, a next-generation fabric technology optimized for HPC deployments. Intel also announced new industry collaborations designed to address the challenges of code modernization and the mainstream use of HPC technologies.

Intel Omni-Path Architecture Market Momentum

Intel Omni-Path Architecture (Intel® OPA) is now sampling with OEM system vendors and is expected to be supported in over 100 switches and server platforms at launch¹. Intel OPA is expected to begin shipping in production by end of year.

Intel OPA switch features enabling higher performance and greater scalability, include:

- Up to 30 percent higher messaging rate per switch port compared to InfiniBand alternatives²
- Up to 73 percent higher switch messaging rate per chip compared to InfiniBand alternatives²
- Up to 23 percent lower switch port-to-port latency compared to InfiniBand-based switches³
- Up to 60 percent lower switch fabric latency in medium-to-large clusters than InfiniBand alternatives³

Advanced features such as traffic flow optimization, packet integrity protection and dynamic lane scaling allow for finer-grained control on the fabric level to enable high resiliency, high performance and optimized traffic movement.

To learn more about Intel OPA technical features and benefits, attend the Intel OPA webinar on Monday, July 13, at 3:00 p.m. EDT/9:00 p.m. CEST. [Register](#) for the webinar.

Intel® Modern Code Developer Community

Building on the success of the [Intel Parallel Computing Centers](#), Intel is announcing the [Intel® Modern Code Developer Community](#) to help HPC developers to code for maximum performance on current and future hardware. Targeting over 400,000 HPC-focused developers and partners, the program brings tools, training, knowledge and support to developers worldwide by offering access to a network of elite experts in parallelism and HPC. The broader developer community can now gain the skills needed to unlock the full potential of Intel hardware and enable the next decade of discovery.

Intel is also announcing the “Intel® Modern Code Challenge 2015,” a contest in partnership with CERN and others where HPC developers can make a difference, learn valuable skills and contribute to a social cause.

Intel and HP Expand Accessibility to HPC Solutions

Intel and HP [today announced](#) a high performance computing (HPC) collaboration designed to expand the use of HPC solutions beyond governments and academia to enterprises of all sizes. The purpose-built HP Apollo compute platforms will utilize the Intel HPC scalable system framework, including next-generation Intel® Xeon® processors, the Intel® Xeon Phi™ product family, Intel® Omni-Path Architecture and the Intel® Enterprise Edition of Lustre* software. From oil and gas and financial services to manufacturing and life sciences, the collaboration will provide customers across a wide range of market segments with workload-optimized solutions based on the latest HPC technologies. The systems will help customers process, analyze and manage their data at lower latency and with extreme scale and efficiency to accelerate business insights and scientific discovery. More information is available at www.hp.com/go/hpc.

New Lustre Software Capabilities

Intel will expand its Lustre software capabilities with the upcoming releases of Intel® Cloud Edition for Lustre Software v1.2 and Intel® Enterprise Edition for Lustre Software v2.3. These new editions will offer enhanced features designed to increase the performance, security and ease-of-use of these popular HPC file system solutions. More information is available at <http://www.intel.com/content/www/us/en/software/intel-solutions-for-lustre-software.html>.

Continued TOP500 Momentum

Intel-based systems account for 86 percent of all supercomputers and 95 percent of all new additions, according to the 45th edition of the TOP500 list announced today. In less than three years since the introduction of the first generation Intel Xeon Phi product family, these many-core, coprocessor-based systems now represent 17 percent of the aggregated performance of all TOP500 supercomputers. The complete TOP500 list is available at www.top500.org.

About Intel

Intel (NASDAQ: INTC) is a world leader in computing innovation. The company designs and builds the essential technologies that serve as the foundation for the world's computing devices. As a leader in corporate responsibility and sustainability, Intel also manufactures the world's first commercially available "conflict-free" microprocessors. Additional information about Intel is available at newsroom.intel.com and blogs.intel.com, and about Intel's conflict-free efforts at conflictfree.intel.com. Intel, the Intel logo, Xeon and Intel Xeon Phi and Omni-Path are trademarks of Intel Corporation in the United States and other countries.

* Other names and brands may be claimed as the property of others.

All products, computer systems, dates and figures specified are preliminary based on current expectations, and are subject to change without notice. All projections are provided for informational purposes only. Any difference in system hardware or software design or configuration may affect actual performance.

¹ Source: Intel internal information. Design win count based on OEM and HPC storage vendors who are planning to offer either Intel-branded or custom switch products, along with the total number of OEM platforms that are currently planned to support custom and/or standard Intel® OPA adapters. Design win count as of July 1, 2015 and subject to change without notice based on vendor product plans.

² Based on Prairie River switch silicon maximum MPI messaging rate (48-port chip), compared to Mellanox CS7500 Director Switch and Mellanox SB7700/SB7790 Edge switch product briefs (36-port chip) posted on www.mellanox.com as of July 1, 2015.

³ Latency reductions based on Mellanox CS7500 Director Switch and Mellanox SB7700/SB7790 Edge switch product briefs posted on www.Mellanox.com as of July 1, 2015, compared to Intel® OPA switch port-to-port latency of 100-110ns that was measured data that was calculated from difference between back to back osu_latency test and osu_latency test through one switch hop. 10ns variation due to "near" and "far" ports on an Eldorado Forest switch. All tests performed using Intel® Xeon® E5-2697v3, Turbo Mode enabled. Up to 60% latency reduction is based on a 1024-node cluster in a full bisectional bandwidth (FBB) Fat-Tree configuration (3-tier, 5 total switch hops), using a 48-port switch for Intel Omni-Path cluster and 36-port switch ASIC for either Mellanox or Intel® True Scale clusters. Results have been estimated or simulated using internal Intel analysis or architecture simulation or modeling, and provided to you for informational purposes. Any differences in your system hardware, software or configuration may affect your actual performance.