INTEL NEWS FACT SHEET

Intel Movidius Myriad 2 Vision Processing Unit (VPU)

High-Performance Visual Intelligence with Ultra-Low Power for Drones, Robotics, Virtual Reality and Smart Security Solutions

The Myriad 2 by Movidius, an Intel company, is a vision processing unit (VPU) that provides low-power, high-performance vision processing solutions across various target applications including embedded deep neural networks, pose estimation, 3D depth-sensing, visual inertial odometry and gesture/eye tracking. Key features include:

- **Ultra-Low-Power Design.** For mobile and connected devices where battery life is critical, Myriad 2 provides a way to combine multiple advanced vision algorithms in a low-power profile. Myriad 2 VPUs offer teraflops (trillions of floating-point operations per second) of performance within a nominal 1 watt power envelope. This enables new vision applications in small form factors that could not exist before.
- **High-Performance Processor.** Bringing vision technologies in connected devices closer to the capabilities of human vision is a core driver for the Movidius group. Myriad 2 enables advanced vision applications that are impossible with conventional processors running in power and thermally constrained environments.
- **Programmable Architecture.** The flexibility for device makers to implement differentiated and proprietary applications is fundamental to Myriad 2. Its optimized software libraries give device manufacturers the ability to differentiate, not duplicate, at the core level.
- **Small-Area Footprint.** To conserve space inside mobile, wearable and embedded devices, Myriad 2 was designed with a very small footprint that can easily be integrated into existing products.

Myriad 2 SoC Specifications

As a system-on-chip (SoC) family of devices, Myriad 2 offers significant computational performance and image processing functions within a low-power footprint.

- Heterogeneous, high throughput, multi-core architecture based on:
  - 12 VLIW 128-bit vector SHAVE processors optimized for machine vision
  - Configurable hardware accelerators for image and vision processing, with line-buffers enabling zero local memory access ISP mode
- Support for 16/32-bit floating point and 8/16/32-bit integer operations
- Homogeneous, centralized memory architecture; 2MB of on-chip memory
- 400 GB/sec of sustained internal memory bandwidth
- 256 KB of L2 cache
- Power management: 20 power islands; low-power states
- Nominal 600 MHz operation at 0.9 V
- Rich set of interfaces:
  - 12 MIPI lanes, 1.5 Gbps per lane configurable as CSI-2 or DSI
  - I2C, SPI for control and configuration
  - I2S for audio input
  - Banks of configurable GPIO, PWM
- Advanced low-power 28nm HPC process node