INTEL NEWS FACT SHEET

Intel Showcases Quantum Computing Research Progress At American Physical Society (APS) March Meeting 2018

March, 2018 - Intel established a quantum computing research initiative in 2015 with QuTech. The program spans the entire quantum system from qubit devices to the hardware and software architecture required to control these devices as well as quantum applications. During the American Physical Society (APS) March Meeting in Los Angeles, researchers from Intel shared advancements in quantum computing research. Below is a summary of the technical papers and presentations by Intel and its research collaborators.

Measuring the Renyi Entropy of a Two-site Fermi-Hubbard Model on a Trapped Ion Quantum Computer
When: Session C39: Scaling up Quantum Computers, Monday, March 5, 2018, 5:06 PM–5:18 PM, LACC Room 501B
Presenter: Anne Matsuura (Intel Labs)
Authors: Norbert Linke (University of Maryland); Sonika Johri (Intel Labs); K.A. Landsman (University of Maryland); Caroline Figgatt (University of Maryland); C. Monroe (University of Maryland); Anne Matsuura (Intel Labs)
Abstract: The efficient simulation of correlated quantum systems is the most promising near-term application of quantum computers. Here, we present the calculation of the second Renyi entropy of the ground state of the two-site Fermi-Hubbard model on a 5 qubit programmable quantum computer based on trapped ions. Our work illustrates efficient mapping of the electronic system to the qubit Hilbert space, circuit compilation and implementation on a physical quantum computer, optimized use of finite quantum gate depth, extraction of a non-linear characteristic of a quantum state using the controlled-swap gate, and effective reduction of experimental errors by over 40 percent using a symmetry-based post-selection scheme. Thus, we demonstrate the first scalable measurement of entanglement on a digital quantum computer, which on larger systems will provide insights into many-body quantum systems that are impossible to simulate on classical computers.

300mm Process Line for Qubit Fabrication
When: Session C28: Silicon Spin Qubits, Monday, March 5, 2018, 4:30 PM–4:42 PM, LACC Room:405
Presenter: Hubert C. George (Intel Corporation)
Authors: Hubert C George (Components Research, Intel Corporation), Kanwal Singh (Components Research, Intel Corporation), Ravi Pillarisetty (Components Research, Intel Corporation), Nicole Thomas (Components Research, Intel Corporation), Jelmer Boter (QuTech and Kavli Institute of Nanoscience, TU Delft), Delphine Brousse (QuTech and Netherlands Organization for Applied Research), J.P Dehollain (QuTech and Kavli Institute of Nanoscience, TU Delft), Gabriel Droulers (QuTech and Kavli Institute of Nanoscience, TU Delft), GertJan Eenink (QuTech and Kavli Institute of Nanoscience, TU Delft), Nico Hendrickx (QuTech and Kavli Institute of Nanoscience, TU Delft), Nima Kalhor (QuTech and Kavli Institute of Nanoscience, TU Delft), Nodar Samkharadze (QuTech and Kavli Institute of Nanoscience, TU Delft), Amir Sammak (QuTech and Netherlands Organization for Applied Research), LaReine Yeoh (QuTech and Kavli Institute of Nanoscience, TU Delft), Diego Sabbagh (QuTech and Kavli Institute of Nanoscience, TU Delft), Giordano Scappucci (QuTech and Kavli Institute of Nanoscience, TU Delft), Menno Veldhorst (QuTech and Kavli Institute of Nanoscience, TU Delft), Lieven Vandersypen (QuTech and Kavli Institute of Nanoscience, TU Delft), James Clarke (Components Research, Intel Corporation)

Abstract: The 300mm fabrication process is the backbone for advanced technology nodes in the semiconductor industry. State of the art transistors most complex integration schemes are only possible using the unique patterning capabilities, high quality material deposition, and process control that are maintained at these facilities. Intel is leveraging its 300mm fabrication expertise to create spin qubit circuits for quantum computing applications. This talk will focus on three aspects: materials, integration, and characterization. Intel has established a supply of high quality material which includes highly purified Si-28 for long coherence times. We also have created a multi-mask integration scheme, which involves custom designed masks that allow fabrication of production quality quantum dots and spin qubits alongside reference transistors. We will be discussing some of the preliminary results from the 300 mm fab and lab line such as structures/features variation, which is imperative for qubit devices.

Constant Time Adiabatic Preparation of the Laughlin State
When: Session H39: New Frontiers in Quantum Algorithms, Tuesday, March 6, 2018, 4:42 PM–4:54 PM, LACC Room: 501B
Presenter: Sonika Johri (Intel Corporation)
Authors: Sonika Johri (Intel Corporation); Zlatko Papic (University of Leeds)
Abstract: The Laughlin wavefunction describes the quantum Hall state at filling factor 1/3 and is an example of a strongly correlated topological phase with anyonic excitations. Such systems are of importance in quantum computing because they are protected by a gap to excited states and thus are robust to local noise. We show that the Laughlin state can be adiabatically connected to a product state by tuning a geometric degree of freedom of the system [1]. Furthermore the gap along this pathway is a constant even in the thermodynamic limit indicating that the state can be prepared in constant time for arbitrary system size up to sub-polynomial factors. In particular, we design and optimize a digital quantum circuit that can be used to prepare the Laughlin state for 6 electrons on as few as 16 qubits, which is within the range of near-term quantum hardware [2]. Techniques like this will be essential for digital quantum computers to aid in the understanding and application of many-body topologically ordered states.
[1] S. Johri et al, New Journal of Physics 18 (2), 025011 (2016).
[2] T.E. O'Brien, B. Tarasinski, and L. DiCarlo, NPJ Quantum Information 3, 39 (2017).

Flip Chip Packaging for Superconducting Quantum Computers
When: Session T33: Superconducting Circuits: Design and Packaging, Thursday, March 8, 2018, 8:36 AM–8:48 AM, LACC Room: 408B
Presenter: Adel Elsherbini (Intel Corporation)
Authors: Adel Elsherbini (Components Research, Intel Corporation), Javier Falcon (Assembly Technology Test and Development, Intel Corporation), Jeanette Roberts (Components Research, Intel Corporation), Roman Caudillo (Components Research, Intel Corporation), Stefano Poletto (Kavli Institute of Nanoscience Delft, Delft University of Technology), Ye Seul Nam, (Assembly Technology Test and Development, Intel Corporation), David Michalak (Components Research, Intel Corporation), Lester Lampert (Components Research, Intel Corporation), Zachary Yoscovits (Components Research, Intel Corporation), Joe Saucedo (Assembly Technology Test and Development, Intel Corporation), Alessandro Bruno (Kavli Institute of Nanoscience Delft, Delft University of Technology), James Clarke (Components Research, Intel Corporation), Leonardo DiCarlo
(Kavli Institute of Nanoscience Delft, Delft University of Technology)
Abstract: Superconducting quantum processors are among the most promising qubit technologies currently being investigated. They offer fast gate speeds, repeatable manufacturability and control. However, one of the major challenges is packaging the superconducting chip to enable reliable connection to the higher temperature control electronics while not impacting the qubit performance. Common interconnect technologies being used such as wirebonding and spring loaded pins suffer from

scaling limitations for larger number of qubits. We will discuss the electrical, mechanical and thermal challenges associated with enabling flip chip packaging for superconducting quantum computing. The package design was verified on internally fabricated 5-qubit and 7-qubit surface code quantum chip and showed comparable coherence times to wirebonded packages while enabling orders of magnitude increase in the number of connections in and out of the die and significantly improved microwave cross talk and spurious modes suppression.

Die Design and Fabrication for Flip-Chip-Packaged Superconducting Quantum Processors
When: Session T33: Superconducting Circuits: Design and Packaging, Thursday, March 8, 2018, 8:48 AM–9:00 AM, LACC Room: 408B
Presenter: Roman Caudillo (Intel Corporation)
Authors: Roman Caudillo (Intel Corporation), Zachary Yoscovits (Intel Corporation), Lester Lampert (Intel Corporation), David Michalak (Intel Corporation), Adel Elsherbini (Intel Corporation), Javier Falcon (Intel Corporation), Jeanette Roberts (Intel Corporation), Leonardo DiCarlo (TUD Faculty of Sciences, QuTech), James Clarke (Intel Corporation)
Abstract: Quantum processors based on superconducting materials with transmon qubits present many scale-up fabrication challenges such as spurious resonances from larger cavity sizes needed to accommodate larger die sizes, tighter tolerances needed for fabrication of a multitude of coplanar waveguide (CPW) resonators coupled to individual feedlines, and excellent process control of Josephson Junction (JJ) fabrication for reliable qubit frequency targeting across large areas. Through silicon vias (TSVs) were developed for improvement of RF hygiene to eliminate spurious resonance modes that can occur due to the larger die sizes. The TSVs are superconducting, which enables the connection of the qubit ground plane to the back plane enabling improved grounding during operation in a dilution refrigerator. Superconducting circuit elements are fabricated from a NbN film chosen for its high kinetic inductance and deposited with a state-of the art tool with excellent cross-wafer uniformity. Aluminum JJs are fabricated using angled-evaporation and cross-wafer uniformity and reliability are studied. Under-bump metallization is studied for optimal assembly to a flip-chip package utilizing Indium-based ball grid array (BGA). The design and fabrication are verified on S17 and S49 quantum chips.

Design and Analysis of Superconducting Qubits for Extensible Surface Coding
When: Session S39: Superconducting Circuits: Modeling, Thursday, March 8, 2018, 11:27 AM–11:39 AM, LACC Room: 501B
Presenter: Nadia Haider (QuTech and TNO)
Authors: Nadia Haider (QuTech and TNO), Stefano Poletto (QuTech and Kavli Institute of Nanoscience, Delft University of Technology), Alessandro Bruno (QuTech and Kavli Institute of Nanoscience, Delft University of Technology), David Michalak (Components Research, Intel Corporation), Roman Caudillo (Components Research, Intel Corporation), Nandini Muthusubramanian (QuTech and Kavli Institute of Nanoscience, Delft University of Technology), Ramiro Sagastizabal (QuTech and Kavli Institute of Nanoscience, Delft University of Technology), Brian Tarasinski (QuTech and Kavli Institute of Nanoscience, Delft University of Technology), Cornelis Christiaan Bultink (QuTech and Kavli Institute of Nanoscience, Delft University of Technology), Michiel Adriaan Rol (QuTech and Kavli Institute of Nanoscience, Delft University of Technology), James Clarke (Components Research, Intel Corporation), Leonardo DiCarlo (QuTech and Kavli Institute of Nanoscience, Delft University of Technology)
Abstract: We present the design and the finite-element electromagnetic analysis of superconducting qubits intended for an extensible surface-code architecture. Surface code, a promising architecture for fault-tolerant quantum computing, requires qubits with connectivity to all nearest neighbors. This interconnectivity, when combined with requirements for microwave and flux controllability, fast gating and readout, makes the design of superconducting qubits for surface coding challenging. We present

the design, simulation, and experimental verification of several variants of seven-port high-coherence transmons.

Temperature Dependence of Spin Relaxation and Charge Noise in Silicon Spin Qubits
When: Session S15: Quantum Networks and Open Systems, Thursday, March 8, 2018, 1:15 PM–1:27 PM, LACC Room: 304C
Presenter: Luca Petit (QuTech and Kavli Institute of Nanoscience, TU Delft)
Authors: Luca Petit (QuTech and Kavli Institute of Nanoscience, TU Delft), Jelmer Boter (QuTech and Kavli Institute of Nanoscience, TU Delft), GertJan Eenink (QuTech and Kavli Institute of Nanoscience, TU Delft), Gabriel Droulers (QuTech and Kavli Institute of Nanoscience, TU Delft), Marco Tagliaferri (QuTech and Kavli Institute of Nanoscience, TU Delft), Ruoyi Li (QuTech and Kavli Institute of Nanoscience, TU Delft), David Franke (QuTech and Kavli Institute of Nanoscience, TU Delft), Nicole Thomas (Components Research, Intel Corporation), Jeanette Roberts (Components Research, Intel Corporation), Ravi Pillarisetty (Components Research, Intel Corporation), Payam Amin (Components Research, Intel Corporation), Hubert C George
(Components Research, Intel Corporation), Kanwal Singh (Components Research, Intel Corporation), James Clarke (Components Research, Intel Corporation), Raymond Schouten (QuTech and Kavli Institute of Nanoscience, TU Delft), Slava Dobrovitski (QuTech and Kavli Institute of Nanoscience, TU Delft), Lieven Vandersypen (QuTech and Kavli Institute of Nanoscience, TU Delft), Menno Veldhorst (QuTech and Kavli Institute of Nanoscience, TU Delft)
Abstract: Large-scale quantum computing is pursued by a wide variety of scientific disciplines. While leading solid-state approaches focus on decreasing the operation temperature to almost zero Kelvin, a crucial question is if the available cooling power will then be sufficient to increase the number of qubits to the required thousands or millions.
Here, we work towards hot-qubits, using electron spins in silicon quantum dots, and characterize the temperature dependence of the spin relaxation time and the charge noise. We have fabricated quantum dot devices on isotopically purified silicon that can host up to four qubits in a linear array. We deplete one quantum dot to the single-electron regime and we are able to readout the spin state in single shot mode. We map out the magnetic field and temperature dependence of the spin lifetime, measuring T1 times larger than 1 ms beyond 1 K. From the temperature dependence study we conclude that the relaxation rate at high temperatures is determined by two-phonon Raman transitions, rather than Orbach processes, up to 1 K. We also investigate the effect of temperature on the charge noise, measured as current fluctuations of a SET, and find consistency with a linear temperature dependence up to 4K.

Media Contacts:

Cara Walker
Intel Media Relations
Cara.walker@intel.com
+1 503-696-0831

Clare Carluccio
Interfuse Communications
Clare.Carluccio@interfusecomms.com
+1 646-935-3962

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