INTEL NEWS FACT SHEET

Intel Highlights Engineering Innovation at International Electron Devices Meeting (IEDM) 2018

Nov. 26, 2018 — Intel researchers will present five papers showcasing technology advances and solutions at IEEE's 64th International Electron Devices Meeting Dec. 3-5 in San Francisco. The papers cover a range of subjects, including one on embedded MRAM, highlighted in the 2018 IEDM Tip Sheet as one of the most newsworthy papers of the conference, and an invited paper on 3D NAND, illustrating the breadth and depth of Intel's process technology work. IEDM is a global forum for reporting technological breakthroughs in the areas of semiconductor and electronic device technology, design, manufacturing, physics and modeling.

MRAM as Embedded Non-Volatile Memory Solution for 22FFL FinFET Technology

When: Session 18.1, Tuesday, Dec. 4, 2:20-2:45 p.m. Grand Ballroom A
Presenter: Oleg Golonzka (Intel Logic Technology Development)
Authors: O. Golonzka, J.-G. Alzate, U. Arslan, M. Bohr, P. Bai, J. Brockman, B. Buford, C. Connor, N. Das, B. Doyle, T. Ghani, F. Hamzaoglu, P. Heil, P. Hentges, R. Jahan, D. Kencke, B. Lin, M. Lu, M. Mainuddin, M. Meterelliyoz, P. Nguyen, D. Nikonov, K. O'Brien, J. O'Donnell, K. Oguz, D. Ouellette, J. Park, J. Pellegren, C. Puls, P. Quintero, T. Rahman, A. Romang, M. Sekhar, A. Selarka, M. Seth, A. J. Smith, A. K. Smith, L. Wei, C. Wiegand, Z. Zhang and K. Fischer, Intel Corporation
Abstract:
This paper is highlighted in the 2018 IEDM Tip Sheet as one of the most newsworthy papers of the conference.
The paper presents key features of production-ready Magnetoresistive RAM-based non-volatile memory (NVM) embedded into Intel's 22FFL FinFET technology. Among other applications, MRAM-based e-NVM is a potential solution for IoT, FPGAs and chipsets with on-chip boot data requirements. Existing solutions – external and embedded flash – suffer from latency delay and high manufacturing costs, respectively. Key features of Intel's MRAM-based e-NVM:

- 1 transistor-1 resistor cell, 216nm x 225nm
- >200°C 10-year retention capability
- $>10^6$ write endurance
- The Magnetic Tunnel Junction-based memory is embedded between metal 2 and metal 4 of the 22FFL process

Retention and endurance capabilities of this high-yielding technology are shown on 7.2 Mbit arrays and full 300mm wafers.

Intel 22nm FinFET (22FFL) Process Technology for RF and mmWave Applications and Circuit Design Optimization for FinFET Technology

When: Session 14.1, Tuesday, Dec. 4, 9:05-9:30 a.m. Continental Ballroom 5
Presenter: Hyung-Jin Lee (Intel Logic Technology Development)
Authors: H.-J. Lee, S. Rami, S. Ravikumar, V. Neeli, K. Phoa, B. Sell, and Y. Zhang, Intel Corporation
Abstract:
Intel's 22nm FinFET (22FFL) process technology is optimized for RF and mmWave applications. Highlights of this paper:

- Describes that 22FFL supports both RF and mmWave applications with best-in-class f_t and f_{max} of NMOS above 300 GHz and 450 GHz, respectively

- Discusses flicker noise improvement over planar technologies and excellent gain-power efficiency to enable low-power wireless applications
- Presents design methodologies to exploit advantages of FinFET technology for RF and mmWave applications

Design-Technology Co-Optimization of Standard Cell Libraries on Intel 10nm Process

When: Session 28.2, Wednesday, Dec. 5, 9:30-9:55 a.m. Grand Ballroom B
Presenter: Xinning Wang (Intel Logic Technology Development)
Authors: X. Wang, R. Kumar, S. Bangalore Prakash, P. Zheng, T.-H. Wu, Q. Shi, M. Nabors, S. C. Gadigatla, S. Realov, C.-H. Chen, Y. Zhang, K. Mistry, A. Yeoh, I. Post, C. Auth, A. Madhavan, Intel Corporation
Abstract:
This paper highlights the co-optimization of process technology, standard cell library offerings and block-level tool-flow-methodology on Intel's 10nm node to enable unprecedented scaling opportunity for products ranging from high performance client/server to low power mobile/IoT segments. The 10nm short height library enables a 2.7x transistor density scaling from the 14nm counterpart. Taller height libraries are optimized to meet performance and reliability requirements of Intel's leading-edge client/server products. Power-performance-area tradeoffs are analyzed at both the standard cell and block level on an industry standard Core IP design.

Scaling Trends in NAND Flash

When: Session 2.1, Monday, Dec. 3, 1:35-2:00 p.m. Grand Ballroom A
Presenter: Krishna Parat (Intel Non-Volatile Memory Solutions Group)
Authors: K. Parat and A. Goda*, Intel Corporation, *Micron Technology
Abstract:
This invited paper describes the evolution of 3D NAND, the current state and future scaling challenges.

- After 2D NAND scaling plateaued due to physical and electrical limitations, the scaling has been continued by migrating to 3D NAND.
- Successive generations of 3D NAND have been delivered with the number of layers now reaching 96 active layers.
- Placing all the CMOS support circuitry under the NAND array has been leveraged to maximize the Gb/mm2 areal densities.
- 4 bits/cell capability is another significant scaling breakthrough providing 33 percent higher Gb/mm2 areal density compared to 3 bits/cell.
- 3D NAND scaling will continue from increasing the number of layers. Key process challenges will be memory hole etching, cell formation in the high aspect ratio memory holes, and improved channel conductivity.

Qubit Device Integration Using Advanced Semiconductor Manufacturing Process Technology

When: Session 6.3, Monday, Dec. 3, 2:25-2:50 p.m. Continental Ballroom 5
Presenter: Ravi Pillarisetty (Intel Components Research)
Authors: R. Pillarisetty, N. Thomas, H.C. George, K. Singh, J. Roberts, L. Lampert, P. Amin, T.F. Watson, G. Zheng, J. Torres, M. Metz, R. Kotlyar, P. Keys, J.M. Boter*, J.P. Dehollain*, G. Droulers*, G. Eenink*, R. Li*, L. Massa*, D. Sabbagh*, N. Samkharadze*, C. Volk*, B. P. Wuetz*, A.-M. Zwerver*, M. Veldhorst*, G. Scappucci*, L.M.K. Vandersypen*, J.S. Clarke Intel Corporation, *TU Delft
Abstract:

INTEL NEWS FACT SHEET

Quantum computing is an emerging technology with the potential for an exponential compute speedup for certain applications. We will discuss our effort to utilize state-of-the-art manufacturing techniques for quantum computing research. Intel leveraged its expertise in transistor process technology to create a 300mm high-volume fabrication and e-test line for semiconductor spin qubits.

About Intel
Intel (NASDAQ: INTC), a leader in the semiconductor industry, is shaping the data-centric future with computing and communications technology that is the foundation of the world's innovations. The company's engineering expertise is helping address the world's greatest challenges as well as helping secure, power and connect billions of devices and the infrastructure of the smart, connected world – from the cloud to the network to the edge and everything in between. Find more information about Intel at newsroom.intel.com and intel.com.