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DCG

Novel Memory/Storage Solutions for Memory-Centric Computing
Mohamed Arafa, Intel, Chandler, AZ – 11:25 AM

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1.4 5G Wireless Communication: An Inflection Point – 11:15 AM
Vida Ilderem, Intel, Hillsboro, OR

The 5G era is upon us, ushering in new opportunities for technology innovation across the computing and connectivity landscape. 5G presents an inflection point where wireless communication technology is driven by application and expected use cases, and where the network will set the stage for data-rich services and sophisticated cloud apps, delivered faster and with lower latency. This paper will highlight the disruptive architectures and technology innovations required to make 5G and beyond a reality.

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2.4 A Distributed Autonomous and Collaborative Multi-Robot System Featuring a Low-Power Robot SoC in 22nm CMOS for Integrated Battery-Powered Minibots

V. Honkote[1], D. Kurian[1], S. Muthukumar[1], D. Ghosh[1], S. Yada[1], K. Jain[1], B. Jackson[2], I. Klotchkov[2], M. R. Nimmagadda[1], S. Dattawadkar[1], P. Deshmukh[1], A. Gupta[1], J. Timbadiya[1], R. Pali[1], K. Narayanan[1], S. Soni[1], S. Chhabra[1], P. Dhama[1], N. Sreenivasulu[1], J. Kollikunnel[1], S. Kadavakollu[1], V. D. Sivaraj[1], P. Aseron[2], L. Azarenkov[2], N. Robinson[2], A. Radhakrishnan[3], M. Moiseev[2], G. Nandakumar[1], A. Madhukumar[4], R. Popov[2], K. P. Sahu[1], R. Peguvandla[1], A. Del Rio Ruiz[3], M. Bhartiya[1], A. Srinivasan[2], V. De[2]
[1]Intel, Bangalore, India; [2]Intel, Hillsboro, OR; [3]Intel, Guadalajara, Mexico, [4]Intel, Toronto, Canada

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8.1 A 93.8% Peak Efficiency, 5V-Input, 10A Max ILOAD Flying Capacitor Multilevel Converter in 22nm CMOS Featuring Wide Output Voltage Range and Flying Capacitor Precharging

C.Schaef[1], S. Weng[1], B. Choi[2], W. Lambert[2], K. Radhakrishnan[2], K. Ravichandran[1], J. Tschanz[1], V. De[1]
[1]Intel, Hillsboro, OR, [2]Intel, Chandler, AZ

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8.5 A Fully Integrated Voltage Regulator in 14nm CMOS with Package Embedded Air-Core Inductor Featuring Self-Trimmed, Digitally Controlled Variable On-Time Discontinuous Conduction Mode Operation

C.Schaef[1], N. Desai[1], H. Krishnamurthy[1], S. Weng[1], H. Do[2], W. Lambert[2], K. Radhakrishnan[2], K. Ravichandran[1], J. Tschanz[1], V. De[1]
[1]Intel, Hillsboro, OR; [2]Intel, Chandler, AZ

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9.6 A 42.2Gb/s 4.3pJ/b 60GHz Digital Transmitter with 12b/Symbol Polarization MIMO

C.Thakkar, S. Shopov, A. Chakrabarti, S. Yamada, D. Choudhury, J. Jaussi, B. Casper
Intel, Hillsboro, OR

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9.7 A Scalable 71-to-76GHz 64-Element Phased-Array Transceiver Module with 2×2 Direct-Conversion IC in 22nm FinFET CMOS Technology

S.Pellerano[1], S. Callender[1], W. Shin[1], Y. Wang[2], S. Kundu[1], A. Agrawal[1], P. Sagazio[1], B. Carlton[1], F. Sheikh[1], A. Amadjikpe[1], W. Lambert[3], D. S. Vemparala[1], M. Chakravorti[1], S.Suzuki[1], R. Flory[1], C. Hull[1]
[1]Intel, Hillsboro, OR; [2]Hillsboro, OR; [3]Intel, Chandler, AZ

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13.2 A 3.6Mb 10.1Mb/mm2 Embedded Non-Volatile ReRAM Macro in 22nm FinFET Technology with Adaptive Forming/Set/Reset Schemes Yielding Down to 0.5V with Sensing Time of 5ns at 0.7V

P. Jain, U. Arslan, M. Sekhar, B. C. Lin, L. Wei, T. Sahu, J. Alzate-vinasco, A. Vangapaty, M. Meterelliyoz, N. Strutt, A. B. Chen, P. Hentges, P. A. Quintero, C. Connor, O. Golonzka, K. Fischer, F. Hamzaoglu
Intel, Hillsboro, OR

TMG

13.3 A 7Mb STT-MRAM in 22FFL FinFET Technology with 4ns Read Sensing Time at 0.9V Using Write-Verify-Write Scheme and Offset-Cancellation Sensing Technique

L. Wei, J. G. Alzate, U. Arslan, J. Brockman, N. Das, K. Fischer, T. Ghani, O. Golonzka, P. Hentges, R. Jahan, P. Jain, B. Lin, M. Meterelliyoz, J. ODonnell, C. Puls, P. Quintero, T. Sahu, M. Sekhar, A. Vangapaty, C. Wiegand, F. Hamzaoglu
Intel, Hillsboro, OR

Intel Labs

14.7 A Modular Hybrid LDO with Fast Load-Transient Response and Programmable PSRR in 14nm CMOS Featuring Dynamic Clamp Tuning and Time-Constant Compensation

X. Liu, H. K. Krishnamurthy, T. Na, S. Weng, K. Z. Ahmed, K. Ravichandran, J. Tschanz, V. De
Intel, Hillsboro, OR

SEG

19.5 Digital Leakage Compensation for a Low-Power and Low-Jitter 0.5-to-5GHz PLL in 10nm FinFET CMOS Technology

Y. Fan, B. Xiang, D. Zhang, J. S. Ayers, K-Y. J. Shen, A. Mezhiba
Intel, Hillsboro, OR

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21.5 A 5G Sub-6GHz Zero-IF and mm-Wave IF Transceiver with MIMO and Carrier Aggregation

B. Jann[1], G. Chance[2], A. Guha Roy[1], A. Balakrishnan[1], N. Karandikar[2], T. Brown[1], X. Li[2], B. Davis[2], J. L. Ceballos[3], N. Tanzi[2], K. Hausmann[2], H. Yoon[2], Y-L. Huang[2], A. Freiman[4], B. Geren[2], P. Pawliuk[2], W. Ballantyne[2]
[1]Intel, Hillsboro, OR; [2]Intel, Chandler, AZ; [3]Intel, Villach, Austria, [4]Intel, Santa Clara, CA

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21.7 A Mixed-Signal Circuit Technique for Cancellation of Multiple Modulated Spurs in 4G/5G Carrier-Aggregation Transceivers

S.Sadjina[1,2], K. Dufrêne[1], R. S. Kanumalli[1], M. Huemer[2], H. Pretl[1,2]
[1]Intel DMCE, Linz, Austria; [2]Johannes Kepler University, Linz, Austria

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25.3 A 128b AES Engine with Higher Resistance to Power and Electromagnetic Side-Channel Attacks Enabled by a Security-Aware Integrated All-Digital Low-Dropout Regulator

A. Singh[1], M. Kar[2], S. Mathew[2], A. Rajan[2], V. De[2], S. Mukhopadhyay[1]
[1]Georgia Institute of Technology, Atlanta, GA, [2]Intel, Hillsboro, OR

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30.4 A 32Gb/s 2.9pJ/b Transceiver for Sequence-Coded PAM-4 Signaling with 4-to-6dB SNR Gain in 28nm FDSOI CMOS

Aurangozeb[1], C. Dick[1], M. Mohammad[2], M. Hossain[1]
[1]University of Alberta, Edmonton, Canada; [2]Intel, Santa Clara, CA

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Applying Principles of Neural Computation for Efficient Learning in Silicon – 2:00 PM

Mike Davies
Intel Labs, Hillsboro, OR

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Design Techniques for a 112Gb/s PAM-4 Transmitter – 10:00 AM

Jihwan Kim
Intel, Hillsboro, OR

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