LAKEFIELD: HYBRID CORES IN 3D PACKAGE

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LAKEFIELD: DESIGN GOALS

• High level goal:
  • Enable new class of compute devices in Mobility form factor (converged Mobility)
  • Best in class Compute performance in lower TDP
  • Always on, always connected, very low standby Power

• What this meant to Compute SOC
  • Migrate to latest Process technology/ Intel 10nm
  • Significant Gen over Gen improvements:
    • ~1/10th Standby Power
    • ~50% GFX improvement
    • ~40% Core area reduction
    • ~40% Z reduction

• How do you achieve this in 1 Generation?
  • Birth of Lakefield!
LAKEFIELD BIG PICTURE: SMALL FORM FACTOR DEVICES

POP PACKAGE: 12.00 x 12.00 MM

12.00 mm Package

12.0 mm Package

1.00 mm Post SMT
LAKEFIELD VS PREV GEN VS COMP

KEY ENABLING VECTORS

SoC
- Hybrid CPU architecture

Package
- 3D Foveros packaging

PCB
- Compact 30x123mm LKF motherboard design
- 0.6mm, 10L, ALV, complete single sided

EC
- EC-lite architecture

Boot
- SPI-less boot from UFS

Form factors
- Dual/foldable displays; thin clamshells
## CORE AREA ATTRIBUTES

<table>
<thead>
<tr>
<th></th>
<th>Y SKU Gen-1</th>
<th>Y SKU</th>
<th>LKF</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Core area attributes</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Core</td>
<td>1x</td>
<td>0.9x</td>
<td>0.4x</td>
</tr>
<tr>
<td>Package</td>
<td>20.5x16.5</td>
<td>26.5x18.5</td>
<td>12x12</td>
</tr>
<tr>
<td>Memory</td>
<td>LP3 11x11.5</td>
<td>LP4-4x 12.5x12.5</td>
<td>LP4-4x POP</td>
</tr>
<tr>
<td>Power Delivery</td>
<td>Discrete VR</td>
<td>FIVR/ Discrete VR</td>
<td>PMIC</td>
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</tbody>
</table>
LAKEFIELD ARCH: HYBRID CORES + 3D DIE STACKING

Latest Display core 4 pipes, 5k60 or 4k120

Latest GFX core Gen 11 64EUs

Latest Media core 4k60/8k30

New Hybrid IA cores 1x SNC + 4x TNT

Latest IPU5.5, up to 16MP, x6 connected cameras

Compute die: 10nm

Base die: P1222
No single transistor node is optimal across all design points!
## INTEL PROCESS DEVELOPMENT MODEL W/ FOVEROS

### LAKEFIELD IMPLEMENTATION

<table>
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<tr>
<th>Manufacturing</th>
<th>Development</th>
<th>Path finding</th>
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<tr>
<td>1274(10nm)</td>
<td>1276(7nm)</td>
<td>1278</td>
</tr>
<tr>
<td>P1222</td>
<td>1274.FV</td>
<td>1276.FV</td>
</tr>
</tbody>
</table>

### Optimized for Compute
- Ultra-Mobile form factor (12x12x1 mm package)
- ~2.x mW Standby Battery Life
- Leadership CPU Performance

### “FOVEROS”
- Mix and Match of IP and process nodes.
- Highest Performance & Lowest Leakage
- Allows IPs to be developed independently, faster time to market

- Optimized X/Y, board area
LAKEFIELD FOVEROS

HIGH BANDWIDTH, ULTRA LOW POWER CONNECTIVITY BETWEEN DIES
SCALABLE TSV FOR POWER DELIVERY
HIGH YIELDING PROCESS FOR DIE 2 WAFER ATTACH, THERMAL SOLUTION TO ENABLE 3D STACKING
LAKEFIELD FOVEROS

10 nm compute process for cores and graphics
LAKEFIELD FOVEROS

IN-PACKAGE DRAM

DRAM INTEGRATION IN 1MM Z HEIGHT

COMPUTE

FOVEROS

BASE

PACKAGE
ADVANTAGES OF HYBRID COMPUTE

- Big-Bigger Compute combination, ideal for mobility compute use case
- Heavy compute, bursty workload on SNC core
- Light compute workload on ATOM/Tremont, w/o compromising on performance
- Low power scenarios that are key to Battery life run on Tremont cores
LKF HYBRID POWER PERFORMANCE

SNC Bigger Core delivers
- Single Thread Performance and Efficiency at burst

TNT Efficient Atom cores deliver
- MT perf and core count/area efficiency
- Power Efficiency with realistic workloads
- Battery Life (HoBL)

For more complete information about performance and benchmark results, visit www.intel.com/benchmarks.
IA HYBRID ARCHITECTURE

- Dynamic feedback to the OS/SW on Hybrid Core PnP capabilities
- Performance/responsiveness threads scheduled on SNC core
- Background and threads scheduled on TNT cores
- All cores execute threaded/concurrent applications
Architecture, Process & Design Optimizations
1. IP partitioning between Compute & Base
2. Vnn Removal, LDO removal and low leakage power gating in base die
3. USB and DDR Phy improvement
4. Very Low leakage transistor usage
5. Logic, Memory, and Clock IP Power scaling

For more complete information about performance and benchmark results, visit www.intel.com/benchmarks.
Lakefield GFX performance @7W

- 9th gen GFX: 1.0X
- Manhattan: 1.53X
- 3DMark11: 1.64X
• LKF introduces first in the industry, a product with 3D stacking, and IA hybrid computing
• First PC Compute SOC with dimensions of 12 x 12 x 1 mm, and Standby power of 2.x mW
• LKF designed for lower power, to enable new thin/ form-factors, 2 in 1's, dual-display devices
• LKF architecture has significant improvements over previous generation with ~0.1x S0iX3, ~0.5x PCB Core area and ~1.5x GFX performance
• Silicon is in final phase of production readiness targeting end of Q4'19
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