Ayar Labs

TeraPHY: A Chiplet Technology for Low-Power, High-Bandwidth In-Package Optical I/O

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Dr. Mark Wade
Erik Anderson
Dr. Shahab Ardalan
Pavan Bhargava
Sidney Buchbinder
Dr. Michael Davenport
Dr. John Fini
Dr. Anatoly Khilo
Roy Meade
Dr. Chandru Ramamurthy
Michael Rust
Dr. Forrest Sedgwick
Dr. Vladimir Stojanovic
Dr. Derek Van Orden
Edward Wang
Dr. Chong Zhang
Dr. Chen Sun

Sponsors:
DARPA CHIPS: Andreas Olofsson
DARPA PIPES: Gordon Keeler
ARPA-E ENLITENED: Mike Haney

Sergey Shumarayev
Conor O'Keeffe
Tim T. Hoang
David Kehlet
Dr. Ravi V. Mahajan
Allen Chan
Tina Tran
Outline

1) Motivation: why are we working on this?

2) Intro to integrated optics and core technology

3) Putting it all together: technology demonstrations

4) Leveraging the chiplet ecosystem

5) TeraPHY – the Terabit/s optical PHY

6) Outlook and conclusions
1) Motivation: why are we working on this?

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6) Outlook and conclusions
Long range SerDes ends at 112 Gb/s

A new universal I/O technology is needed
• Severe bandwidth tradeoff versus distance
• Large penalties for leaving the chip package and the board
• ~4 orders of magnitude difference in FoM from in-package to off board!
• Can integrated optics address this gap?

I/O Bandwidth trends

[G. Keeler, DARPA ERI 2019]
I/O Bandwidth trends

- Severe bandwidth tradeoff versus distance
- Large penalties for leaving the chip package and the board
- ~4 orders of magnitude difference in FoM from in-package to off board!
- Can integrated optics address this gap?

[Image: I/O Bandwidth trends diagram]

[G. Keeler, DARPA ERI 2019]
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Silicon photonics building blocks

- Waveguides on chip form photonic circuit building blocks
  - waveguides
Silicon photonics building blocks

- Waveguides on chip form photonic circuit building blocks
  - waveguides
  - directional couplers

Evanescent coupling between waveguides

Mach-Zehnder Interferometer
Silicon photonics building blocks

- Waveguides on chip form photonic circuit building blocks
  - waveguides
  - directional couplers
  - microring resonators

![Diagram showing off-resonance and on-resonance states of a microring resonator with input (IN) and through (THRU) ports. On resonance, there is a drop (DROP) at a specific wavelength.]
MZI’s versus microrings

Microrings offer:
~100x smaller footprint
~25-50x higher bandwidth density
~50x higher energy efficiency
Getting light on and off the chip: vertical grating couplers

cross-sectional view
Getting light on and off the chip: vertical grating couplers
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cross-sectional view
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Microring-based WDM Optical Architecture

- Off-chip light source produces continuous wave (CW) laser
- Light is coupled from fiber-to-chip through vertical grating couplers
- Microring modulator converts data from electrical domain to optical domain
- Microring detector converts data from optical domain to electrical domain
Microring-based WDM Optical Architecture

- Microring modulators act as both a modulator and a wavelength multiplexer
- Microring detectors act as both a detector and wavelength demultiplexer
Microring-based WDM Optical Architecture

- Cascaded microrings along same waveguide increases data per fiber
- Each microring acts as an independent communications channel
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Microring-based WDM Optical Architecture

- Cascaded microrings along same waveguide increases data per fiber
- Each microring acts as an independent communications channel
- Scalable architecture up to ~64 microrings
Building WDM Systems

- Monolithic integration allows for clocking, drivers, TIAs, and control circuitry to be integrated on same chip as optical devices
- Small size of microring devices monolithically integrated with CMOS transistors leads to large bandwidth density and energy efficiency
Putting it together: First CPU with optical I/O

- Single SOI CMOS CPU chip with optical I/O
- 70M transistors
- ~1,000 optical devices
- Microring based WDM

Enabled by the DARPA POEM project

Putting it together: First CPU with optical I/O

Enabled by the DARPA POEM project

Ayar Labs optical I/O architecture

- Monolithic integration allows flexible electrical I/O interface to host SoC
- Wide parallel or high-speed serial
- Silicon interposer or organic substrate
- Remote laser source simplifies packaging
TeraPHY technology test chip

- Includes all electronics and photonics for optical I/O (except laser)
- Transmitter: 2.0 Tbps (5 x 400Gbps)
  - 16 x 25Gbps
  - Digital backend
  - SerDes
  - High-speed clocking, distribution
  - Closed-loop thermal control
  - Built-in self test (BERT, debug, etc.)
- Receiver: 1.2 Tbps (3 x 400Gbps)
  - 16 x 25Gbps
  - Digital backend
  - SerDes
  - PD, TIA, equalization, CDR, clocking

[M. Wade et al., OFC/ECOC 2018]
TeraPHY Technology demonstrations: WDM Tx Macro

- 16 x 25 Gbps
- 1 Tbps/mm
- 1 Tbps/mm$^2$
- 0.8 pJ/bit

[M. Wade et al., ECOC 2018]
TeraPHY Technology demonstrations: WDM Rx Macro

- 1 Tbps/mm
- 500 Gbps/mm²
- 2.5 pJ/bit

Rx Eye Monitor Sweep

Optical Rx BER Measurement

[22 Gbps, 24 Gbps, 25 Gbps]

0.35UI at 25Gbps

[M. Wade et al., ECOC 2018]
TeraPHY Performance

- >500 Gbps/mm², >1 Tbps/mm bandwidth density
- <5 pJ/bit energy efficiency (all-inclusive of optics and circuits)
- Support high-performance SoC's escaping many terabits/second

Monolithic electronic-photonic integration in GlobalFoundries 45nm process

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backend dielectrics and metals
- crystalline silicon waveguide
- polysilicon waveguide
- ridge waveguide
- vertical grating coupler

Monolithic electronic-photonic integration in GlobalFoundries 45nm process
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Industry Adoption of System-in-Package Integration

• Examples:
  • Intel® Agilex™ FPGAs
  • Nvidi Tesla T100
  • Intel® Xeon® Scalable Processor Kaby Lake G
  • AMD Radeon R9 Fury X

• Mix die function
  • GPU, CPU, memory, I/O, etc.

• Diverse processes & nodes
  • E.g. 16nm, 10nm, DRAM, etc.

• Manage yield

• For optics to use ecosystem, must be like electronics!
Embedded Multi-die Interconnect Bridge (EMIB)

- EMIB packaging technology supports mixed bump pitch on the same die
- Embedded silicon bridge is used for dense die-to-die connectivity
- Organic substrate is used for off-package connections (power, I/O, etc.)
Die-to-die interface: Serial vs Parallel

### High-speed serial: 25-112 Gb/s per wire
- **die 1**
- **die 2**

<table>
<thead>
<tr>
<th>Metric</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandwidth density</td>
<td>~1 Tb/s/mm</td>
</tr>
<tr>
<td>Energy</td>
<td>~2 pJ/bit</td>
</tr>
<tr>
<td>Design complexity</td>
<td>high</td>
</tr>
<tr>
<td>Package complexity</td>
<td>low</td>
</tr>
</tbody>
</table>

### Wide parallel: 1-5 Gb/s per wire
- **die 1**
- **die 2**

<table>
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<tr>
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<td>Energy</td>
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<tr>
<td>Design complexity</td>
<td>low</td>
</tr>
<tr>
<td>Package complexity</td>
<td>moderate</td>
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</table>
**Advanced Interconnect Bus (AIB)**

- AIB interface offers a suitable parallel interface and is compatible with both current (Intel® Stratix10™) and next-gen (Intel® AgileX™) FPGAs.

- AIB is open source.

- Parallel in-package (2Gbps/IO)
- At ~3ns latency
- Over 1st gen EMIB (500 IOs/mm)
- At 0.85pJ/bit (for 55um ubump)

FOM=(2Gbpsx500/mm)/(0.85pJ/bit)=1176

S. Shumarayev, DARPA CHIPS, 2019
Bringing it all together: TeraPHY + EMIB + AIB + FPGA

Chiplet Integration Platform
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TeraPHY: Main features

- 24 Channels of AIB (960 Gbps total data bandwidth)
- 10 photonics Tx/Rx macro pairs
- Configurable to 128 – 256 Gb/s per macro (1.28-2.56 Tb/s per chip)
- NRZ modulation format on the optical channel – no FEC required!
- <10 ns (AIB -> TeraPHY -> AIB) + 5 ns/m latency
- Configurable cross-bar to map AIB channels to optical channels
- Reach: Up to 2km
- Estimated energy efficiency: <5 pJ/bit (all-inclusive)
TeraPHY: Main features

Physical Implementation
TeraPHY: Physical layout

- AIB interface
- AIB-to-TeraPHY macro crossbar
- Optical input/output
- TeraPHY macros
AIB
Fiber Array
RX
TIA, EQ
Clock
I/Q Gen.
ILO
3 X PI
3 X PI
I/Q Gen.
ILO
Clock
I/Q Gen.
ILO
TX
Eye Monitor
Heat Driver

Tx/Rx Slice
EMIB Substrate

EMIB Link between TeraPHY and FPGA

TeraPHY Location
SoC package assembly
Logically connected, physically distributed

- TeraPHY based optical fabric creates new opportunities to build high bandwidth, low latency connectivity straight from the package
- Enables shelf, rack, and row system scale out
Conclusions

- Chip-to-chip communications requires photonics to overcome I/O bottleneck
- Emerging chiplet ecosystem offers opportunity for in-package optics
- In-package optics fundamentally breaks the traditional bandwidth-distance trade-off and supports new high-performance computer architectures
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