Tremont: Top-level Design Targets

Single thread performance

Networking
- Performance/mW
- Performance/mm²
- New instructions

Battery life
- Performance/mW
Design Target: Single Thread Performance

- Intel® Core™ class branch prediction
- 6 wide out of order instruction decode
- 4 wide allocation
- 10 execution ports
- Dual load/store pipelines
- Quad-core module
- L2 cache up to 4.5MB
  - Size is product dependent
Front End
Front End: Fetch, Predict

Core™ class branch prediction
- Long history
- 32 byte based
- L1 predictor (no penalty)
- Large L2 predictor

Out of order fetch
- 32KB instruction cache
- 32 bytes / cycle
- Up to 8 outstanding misses
Front End: Decode

6-wide x86 instruction decode
- Dual 3-wide clusters
- Out of order
- Wide decode without the area of a uop cache
- Optional single cluster mode based on product targets
Integer Execution

Large entry out of order window (>200)
Parallel reservation stations (6)
Wide execution (7)
  - 3 ALU
  - 2 AGU
  - 1 jump
  - 1 store data
Vector Execution

Crypto acceleration
- Dual 128b AES units, 4 cycle
- Single instruction SHA256, 4 cycle
- Galois Field new instructions

Parallel reservation stations (2)

Execution ports (3)
- SIMD/AES/FMUL
- SIMD/AES/FADD
- Store data
Memory Execution

- Dual load/store pipeline
- 32KB data cache
  - Three cycle load to use
- 1024 entry second level TLB
  - Shared between code and data
Memory Subsystem

L2 shared among 1-4 cores
- Configurable from 1.5MB to 4.5MB

Last level cache support
- Inclusive
- Non-inclusive

Intel® Resource Directory Technology
- L2 QoS including code/data prioritization
- LLC QoS
- Memory bandwidth enforcement
New Instructions and Technologies

Accelerator interfacing Instructions
- Efficient and scalable work-dispatch and synchronization to accelerators

Intel® Speed Shift
- Improved responsiveness with faster hardware controlled frequency changes

CPU rooted secure boot
- Intel® Trusted Execution Technology
- Intel® Boot Guard

Intel® Total Memory Encryption
- Improve confidentiality protection in memory from physical attacks
ISO-Frequency Single Thread Performance Improvement
(Relative to Goldmont Plus)

Based on performance projections as of October 2019 and subject to change, with SOCs at ISO frequencies
For more information about performance and benchmark results go to www.intel.com/benchmarks.
Performance - Hybrid

Based on pre-silicon projections as presented at Hotchips presentation, August 2019 and subject to change
For more information about performance and benchmark results go to [www.intel.com/benchmarks](http://www.intel.com/benchmarks).
Tremont: Intel’s next generation low power x86 microarchitecture

Advancements on ISA, microarchitecture, security, and power management

Out of order front end and 10 wide execution port back-end

Significant IPC improvement vs. prior Intel low power x86 architectures

Targeting a wide variety of products across client, data center, 5G networking and Internet of Things
NOTICES AND DISCLAIMERS

- Performance results for ISO Frequency Single thread performance are performance projections based on preliminary development board measurements as of October 2019 and subject to change. Performance results for hybrid performance are based on pre-silicon projections as of August 2019 and are subject to change, may not reflect all publicly available security updates. No product can be absolutely secure.

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